EV317195787

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

# 23/E 8/5/3

M .	0/20
plication Serial No	09/875,501 /Jul
Filing Date	June 4, 2001 <sup>C</sup>
Inventor	
Assignee	Micron Technology, Inc.
Group Art Unit	
Examiner	E. Ortiz
Attorney's Docket No	
Title: Methods for Forming Wordlines, Transistor Interconnects, and Wordline, Transistor Gate, an	Gates, and Conductive
Structures	

## RESPONSE TO MARCH 19, 2003 FINAL OFFICE ACTION ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION (RCE)

To:

Mail Stop RCE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

From:

D. Brent Kenady

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Wells St. John P.S.

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Spokane, WA 99201-3828

Responsive to the Final Office Action dated March 19, 2003, Applicant amends and remarks as follows:

## **AMENDMENTS**

<u>Underlines</u> indicate insertions and strikeouts indicate deletions.